

**Notice of References Cited**

Application/Control No.

09/668,320

Applicant(s)/Patent Under  
Reexamination  
ALPERT ET AL.

Examiner

Morella I Rosales-Hanner

Art Unit

2128

Page 1 of 2

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,347,393	02-2002	Alpert et al.	716/2
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Curtis L. Ratzlaff, Satyamurthy Pullela and Lawrence T. Pillage, "Modeling the RC-Interconnect Effects in a Hierarchical Timing Analyzer", IEEE 1992 Custom Integrated Circuits Conference, Pgs 15.6.1 - 15.6.4.□□
	V	Andrew B. Kahng and Sudhakar Muddu, "Two-pole Analysis of Interconnection Trees", 1994 IEEE, Pgs 105 - 110.□□
	W	Charles J. Alpert, Anirudh Devgan and Stephen T. Quay, "Buffer Insertion with Accurate Gate and Interconnect Delay Computation", DAC '99, Pgs 479 - 484□□
	X	Charles J. Alpert, Anirudh Devgan and Stephen T. Quay, "Buffer Insertion for Noise and Delay Optimization", IEEE transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol 18, No.11, Nov 1999, Pgs 1633 - 1645□□

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<b>Notice of References Cited</b>	Application/Control No. 09/668,320	Applicant(s)/Patent Under Reexamination ALPERT ET AL.	
	Examiner Morella I Rosales-Hanner	Art Unit 2128	Page 2 of 2

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	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Jessica Qian, Satyamurthy Pullela and Lawrence Pillage, "Modeling the "Effective Capacitance" for the RC Interconnect of CMOS Gates", IEEE transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol.13, No.12, Dec 1994, Pgs 1526 - 1535
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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